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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/706,274	11/03/2000	Susanne Arney	ARNEY 8-51-1	6293

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EXAMINER	
SODERQUIST, ARLEN	

ART UNIT	PAPER NUMBER
1743	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/706,274	ARNEY ET AL.
	Examiner	Art Unit
	Arlen Soderquist	1743

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16,18-31 and 33-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13-16,18-26,28-31,33-41 and 43-45* is/are rejected.

7)☒ Claim(s) *12,27 and 42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims 1-5, 7-11, 14, 16, 18-20, 22-26 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Enlow or Murphy (newly cited and applied) in view of Shanefield or Vaidya (newly cited and applied).

In the paper Enlow discusses development of test vehicles for evaluating plastic-encapsulant reliability and improving thermal conductivity of encapsulant materials. Plastic-encapsulated microcircuits (PEMs) are proposed for use in military systems. PEMs reduce cost and eliminate long-lead items such as packages and lids. Encapsulant materials must be evaluated for compatibility with devices and fine-wire bonds, and electrical stability on deposited elements and integrated-circuit devices. Reliability evaluations in screen tests and various temperature/humidity/bias environments are also essential prior to use in advanced packaging. Encapsulant reliability evaluation requires a test vehicle (MCM-C and MCM-L) to identify these key performance characteristics. Commercial off-the-shelf parts that may be sensitive to encapsulant screening are transistor devices or PROM parts that can be tested for leakage currents, or programmed and verified. No complete multichip test vehicle, however, is available for use. An encapsulant test vehicle with three unpassivated resistor networks used in previous work was modified by substituting a Sandia ATC04 chip and a silver-comb-pattern array with varying feature sizes (2-, 5-, 17- and 25- m lines and spaces) and using only a single nichrome-resistor network (pages 315-316). Finally, a deposited comb pattern was added. The

remaining single unpassivated resistor and a silver-comb pattern offer both a go/no-go and quantitative test for screening encapsulants. See the second paragraph of page 316 for teachings regarding the comb patterns of varying lines/spaces providing quantitative as well as a go/no-go status. Use of the Sandia chip facilitates stress measurements on the die as well as thermal dissipation evaluation with resistance heaters on the chip. An industry-standard encapsulant, Hysol FP 4450, was modified by substitution of silica-coated aluminum nitride or boron nitride and spherical alumina fillers for the standard silica fillers. Other components in the material are a blend of epoxy resins and an aromatic anhydride hardener. Exact filler selection and loading were optimized, balancing dispensability, wear, and flow characteristics. Control materials (Hysol FP 4450) and improved, thermally conductive versions were exposed to short-term screen tests, long-term temperature cycling, humidity cycling, and elevated temperature storage testing. The set of comb electrodes of varying sizes and spacings as shown in figure 3b meets the limitations of the rejected claims in that the comb patterns with narrower spacing inherently oxidize at a rate greater that the electrical component (combs with the larger spacing). This inherent property results in the go/no-go and quantitative results taught on page 316. Enlow does not teach the sensor trace having a meandering pattern and located between two grounded conductors on the insulating substrate.

In the paper Murphy presents an evaluation of non-hermetic coatings for MCM applications through HAST, 85/85 and PCT. The goal of the Reliability without Hermeticity (RwoH) Project is to find non-hermetic coatings for use on MCMs. As a means of down-selecting coating materials, Sandia Assembly Test Chips (ATC01) test chips in 40 pin DIPs were coated with non-hermetic, polymer materials, including silicone gel, filled epoxy, and polyimide. After preconditioning through temperature cycling and salt atmosphere, the parts were subjected to one of three different temperature, humidity, and bias conditions: HAST (140 C, 85% RH, +40V), 85/85 (85 C, 85% RH, +40V), or PCT (121 C, 99.6% RH). No universal relationship between lifetime in HAST and 85/85 testing was observed--the effects appear to be material dependent. Electrical test data suggest that failures on coated parts (with standard SiN chip passivation) do not occur on die circuitry (triple tracks) and instead occur on bond-wires and bond-pads. In the approach section starting on page 339, figure 1 and table 1 the ATC01 used was described to include four different triple track test structures with line width and line

spacings from 2-6 μm. The different line widths and spacings as shown in Table 1 meet the limitations of the rejected claims in that the patterns with narrower spacing inherently oxidize at a rate greater that the electrical component (patterns or test structures with the larger spacing). Murphy does not teach the central trace being biased positively relative to the two outer conductors.

In the paper Shanefield discusses a proposed standard environmental test of component coatings. Committee S-32-1 of the IEEE has been formed to suggest a standard testing procedure for coatings used to protect electronic components. This procedure is expected to be issued as an IEEE Standard. The procedure involves any of three test devices: thin film resistors, thick film resistors, or a silicon IC. Each of these has 'triple track' patterns with three parallel conductive lines, folded back and forth many times (serpentine shape) to cover the surface efficiently. The test device is cleaned, coated with the material to be tested, and placed in an oven at 85 °C and 85% relative humidity. An appropriate voltage is imposed between the center conductive line and the outer two grounded lines. Any small electric current ('leakage') is monitored for 1000 hrs, and continuity of the lines is also checked periodically, to detect possible corrosion. A high quality protective coating will provide low leakage currents and no open circuits. Page 72 on the first paragraph discusses the triple track conductor setup for a silicon IC device including the conductors being made of an aluminum alloy that contains a small mount of copper and silicon. The testing conditions are also found on page 72 including the recommended voltages for the biasing. In the second paragraph of the introduction Shanefield discusses the various tests in us to test the encapsulant and teaches that their parameters are only indirectly related to reliability, resulting in the formation of the committee to suggest a more relevant test procedure.

In the paper Vaidya discusses electromigration resistance of fine-line aluminum for VLSI applications. The electromigration lifetimes were determined for an as-yet unexplored combination of long lines (≤3 cm) and narrow linewidths (≥1 μm) of evaporated and magnetron sputter-source deposited Al-Cu-Si films. The lifetimes for the sputtered films are significantly smaller than those for electron-beam evaporated films. The latter displayed an unusually large improvement in the lifetime for finer linewidths (1.5 and 1 μm). Failure modes were analyzed

and correlations made with a new microstructural parameter incorporating the film grain-size, its sigma and the degree of preferred orientation. Figure 1 shows that testing structure used to be a comb structure with a meander interspersed therebetween. Page 165 in the description of the test structure teaches the combs as not powered. In the second paragraph of the test structure section Vaidya teaches that the structure used was a departure from previous structures and was "motivated by a desire to make the testers approximate more closely the VLSI device dimensions".

It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the Enlow device to conform to the standard test structure proposed in the Shanefield article or include a meander trace as taught in the Vaidya article because of the fact that Shanefield is presenting a standard that as taught by Shanefield will be a more relevant procedure in determining the performance of the device or as Vaidya teaches was motivated by a desire to have the testers be a better approximation of the device dimensions. It would have been obvious to one of ordinary skill in the art at the time the invention was made to bias the test structures of Murphy as taught by Shanefield or Vaidya because Shanefield is presenting a standard method or device that as taught by Shanefield will be a more relevant procedure in determining the performance of the device or as Vaidya teaches was motivated by a desire to have the testers be a better approximation of the device dimensions.

3. Claims 6 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Enlow or Murphy in view of Shanefield or Vaidya as applied to claims 1 or 16 above, and further in view of Gabriel full article newly cited and applied) or Ziaie. Enlow and Murphy do not teach the sensor trace made of silicon.

In the paper Gabriel teaches detection and prevention of polysilicon filaments along field oxide isolation edges. When current leakage was detected between tightly spaced polycide gates, SEM micrographs revealed polysilicon filaments caused by residual polysilicon filling a notch at the field oxide edge. A test structure with interdigitated polysilicon lines having variable spacing over severe LOCOS topography was designed to allow rapid detection of such polysilicon filaments. The test structure was used to optimize polysilicon overetch time. The minimum overetch time required to prevent filament formation depends on the spacing between lines and on LOCOS isolation processing parameters. Page 282 teaches in the first paragraph of

the experimental section that the interdigitated comb test structure polycide line spacings vary from 0.45 to 1.8 μm.

In the paper Ziaie teaches a hermetic glass-silicon micropackage with high-density on-chip feedthroughs for sensors and actuators. This paper describes the development of a hermetic micropackage with high-density on-chip feedthroughs for sensor and actuator applications. The packaging technique uses low-temperature (320 °C) electrostatic bonding of a custom-made glass capsule (Corning #7740, 2×2×8 mm3) to fine grain polysilicon to form a hermetically sealed cavity. High-density on-chip multiple polysilicon feedthroughs (200 per mm) were used for connecting external sensors and actuators to the electronic circuitry inside the package. A high degree of planarity over feedthrough areas was obtained by using grid-shaped polysilicon feedthrough lines that are covered with phosphosilicate glass (PSG), which is subsequently reflown at 1100 °C in steam for 2 hours. Saline and DI H_2O soak tests at elevated temperatures (85 and 95 °C) were performed to determine the reliability of the package. Preliminary results showed a mean time to failure (MTTF) of 284 days and 118 days at 85 and 95 °C, respectively, in DI H_2O. An Arrhenius diffusion model for moisture penetration yields an expected lifetime of 116 yr at body temperature (37 °C) for these packages. In vivo tests in guinea pigs and rats for periods ranging from one to two months showed no sign of infection, inflammation, or tissue abnormality around the implanted package.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the Enlow or Murphy sensor trace out of silicon as taught by Gabriel or Ziaie because of the ability to test for problems in polysilicon as taught by Gabriel and Ziaie.

4. Claims 5, 13, 15, 20, 28, 30-31, 33-35, 37-41 and 43-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Enlow or Murphy in view of Shanefield or Vaidya, as applied to claims 1-5, 7-11, 14, 16, 18-20, 22-26 and 29 above, and further in view of Sweet and Burack, Mancke or Wada (1989). The Enlow and Murphy papers do not teach an integrated circuit including the sensing device or the sensing device trace made from the specifically claimed metals.

In the paper Sweet discusses high reliability plastic packaging for microelectronics. This Laboratory Directed Research and Development (LDRD) project conducted in fiscal years 1996 and 1997 under case 3526.030 was devoted to the development of test structures and associated

measurement methodology for assessing the reliability of plastic encapsulated microelectronic devices. The end goal was the conceptual specification of one or more Assembly Test Chips (ATCs) which could be used evaluating plastic encapsulation technologies. In this work the authors demonstrated suitable circuits for measuring Au-Al wirebond and Al metal corrosion failure rates during accelerated temperature and humidity testing. Also the test circuits on the authors' ATC02.5 chip were very sensitive to extrinsic or processing induced failure rates. A number of accelerated aging experiments were conducted with unpassivated triple track aluminum structures on the ATC02.6 chip to demonstrate that these would be extremely sensitive to environmental conditions. The authors found an unexpected result, the unpassivated tracks were very sensitive to particulate contamination which caused conductor damage and resultant high voltage breakdown. A number of modifications to existing circuitry were suggested as a result of the unpassivated device experiments. Also the piezoresistive stress sensing circuitry which the authors had designed for the ATC04 test chip was suitable for determining the change in the state of mechanical stress at the die when both initial and final measurements were made near room temperature. However, the authors' attempt to measure thermal stress between room temperature and a typical polymer glass transition temperature failed because of excessive die resistor-substrate breakage currents at the high temperature end. Suitable circuitry changes were developed which should eliminate this problem. One temperature and humidity experiment was conducted with Sandia developed static random access memory (SRAM) parts to examine non-corrosion CMOS failures. This experiment did not achieve the desired objective because of processing problems but the authors did demonstrate that the authors could easily detect and measure a new type of corrosion failure mode, this time at the model to Si contacts on the die surface. As a result of this two year effort, the authors have new designs for a number of test circuits which could be used on an advanced ATC for reliability assessment in Defense Programs electronics development projects. In the final paragraph of page 27 Sweet teaches that the next logical step is to demonstrate on model weapons electronics system that a multifunction ATC could detect the presence of potentially damaging environments before actual integrated circuits started to fail.

In the paper Burack discusses enhanced moisture protection of electronic devices by ultrathin polyimide films. Thin films of polyimide which exhibit enhanced resistance to

moisture were fabricated using the Langmuir-Blodgett (LB) technique. The adhesion strength of both LB and spin-coated films of several different polyimides, deposited on fused silica, was measured by subjecting these films to steam or water, followed by a tape test, and monitoring changes in the UV spectra of the films, showing that the LB films of polyimide adhere better to fused silica than spin-coated films. In addition, water vapor transmission rate measurements through Kapton sheet coated by a monolayer of any of the polyimides show that a monolayer forms a moisture barrier, decreasing the water vapor transmission through the Kapton. Based on these results, the electrical performance of polyimide films was tested at 85 °C, 85% humidity, by measuring leakage current between conducting paths (figure 6) under 180-V bias, on samples which were coated with various combinations of LB and spin-coated polyimide films. Composite films of polyimide consisting of a LB monolayer, either underneath or on top of a thick, spin-coated film, exhibited superior electrical performance to either a spin-coated or LB film by itself. This may be explained by the improved adhesion and/or decreased water permeability of polyimide LB films.

In the paper Mancke discusses a moisture protection screening test for hybrid circuit encapsulants. An empirical comparative screening test for polymeric encapsulants was described with respect to figures 1-4 and used to indicate how well different materials prevent unwanted leakage currents between closely spaced biased metal lines in hybrid integrated circuits. The screening test circuit, test procedure, and test conditions are described. This test and measurement equipment was developed earlier by N. L. Sbar and R. P. Kozakiewicz (1977-9). Data for two silicone coatings and one epoxy coating were compared with data for DC 3-6550 RTV. Results are also shown for layers of two different polymer coatings. The coatings of the same general polymer type varied considerably in performance in this screening test.

The Wada paper discusses the influence of passivation layer on aluminum corrosion on simulated microelectronics circuit pattern. The corrosion of thin Al is one of the important failure mechanisms in integrated circuits. Al corrosion and electrolytic leakage current were studied by temperature-humidity-bias tests. Two different passivation layers were investigated: a double layer of nondoped silicate glass (NSG) on phosphosilicate glass (PSG), and single layer of plasma-deposited SiN. Samples were prepared with 3 different combinations of width/spacing: 2/2 μm (width/spacing), 4/4 and 12/6 μm, 2/2 and 4/4 μm patterns with a

passivation layer on the stripes and a 12/6 μm pattern in which a part of the passivation layer is etched to expose the Al stripe. Investigation of these patterns via temperature-humidity-bias tests leads to the following conclusions. With SiN passivation, cathodic Al corrosion did not occur on 2/2 and 4/4 μm patterns. On the other hand, with PSG + NSG passivation, cathodic corrosion occurred on 3 patterns. In 12/6 μm patterns with SiN passivation, the leakage current increased earlier than did that of 2/2 and 4/4 μm SiN passivated patterns. Thus, leakage current is conducted through the interface between the passivation layer and the plastic resin. In a special Al pattern in which a part of SiN passivation layer is etched to expose the stripe, local anodic corrosion was dominant. This anodic corrosion can be explained by the F in CF_4/O_2 plasma used for SiN etching.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the serpentine sensors of Sweet, Burack, Mancke or Wada into the Enlow or Murphy multifunction test chip for their recognized equivalent information regarding failure of conductors for a wide range of metals used in electronic devices. It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the multifunction testing structure into actual integrated circuit packages as taught by Sweet because of their ability to detect environments and other effects that would cause failures of the integrated circuit before the integrated circuit actually fails.

5. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Enlow or Murphy in view of Shanefield or Vaidya and Sweet and Burack, Mancke or Wada (1989) as applied to claim 31 above, and further in view of Gabriel or Ziaie as explained above. Enlow and Murphy do not teach the sensor trace made of silicon.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the Enlow or Murphy sensor traces out of silicon as taught by Gabriel or Ziaie because of the ability to test for problems in polysilicon as taught by Gabriel and Ziaie.

6. Claims 12, 27 and 42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The art does not teach or fairly suggest the respective structures.

7. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection. The Enlow and Murphy references clearly have a structure that is designed to have at least one component oxidize (create a short) before other electrical components in the electronic circuit, the Shanefield reference clearly teaches the triple track format as a standard that removes some of the problems of previous testing procedures and the Vaidya reference clearly teaches that motivation can come from a desire to have the test structure more closely approximate the actual devices. Contrary to applicant's arguments, a standard procedure as is found in the Shanefield article can form a perfectly good reason for making changes so that the testing procedure used conforms to an accepted standard and thereby will be accepted by those that are using the standard as their measurement procedure. One need only look to the newly cited and applied Murphy reference to see that the art recognized that the smaller line widths and spacings produced a more aggressive geometry (created more problems relative to the electrical test structure failure). This understanding/expectation led to the conclusion that the failures that were seen were due to bond pad problems rather than triple track failures with the silicon coating. This expectation also led to a teaching the newly cited Troyk reference in the last paragraph of page 976 that a sample that contained two different line spacings on the same substrate could be used to examine early deterioration of an interface between the substrate and a covering polymer.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The additional art related to detecting failures in electrical devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arlen Soderquist whose current telephone number is (571) 272-1265 as a result of the examiner moving to the new USPTO location. The examiner's schedule is variable between the hours of about 5:30 AM to about 5:00 PM on Monday through Thursday and alternate Fridays.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the examiner at the above telephone number.

Arlen Soderquist

January 5, 2004

ARLEN SODERQUIST
PRIMARY EXAMINER